REMARKS/ARGUMENTS

Claims 1-4 are pending in the Application. Reconsideration and allowance in view of the following remarks are respectfully requested.

In Paragraph 4 which begins on page 2 of the Office Action, claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (Figs. 7-9) in view of EP 0,499,275 of Hojo et al. This rejection is respectfully traversed.

Briefly stated, the present invention provides a charge transfer element comprising a reverse conductive type well formed on the surface of one conductive type semiconductor substrate, the one conductive type channel region extending in one direction relative to the well, a transfer electrode formed intersecting the channel region, a floating diffusion region formed continuous from the channel region, and an output transistor having a gate connected to the floating diffusion region. In a region where the output transistor is formed, the dopant density profile in the depth direction of the semiconductor substrate exhibits the maximum value relative to a middle region.

In rejecting claims 1-4 as unpatentable over Admitted Prior Art (APA) in view of Hojo et al., the Office Action states that APA teaches a charge transfer element, as shown in Fig. 9. Hojo et al. is said to teach a P-Well region having maximum dopant density value relative to a middle region of the P-Well region to function as an overflow barrier. According to the Office Action, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Hojo into APA because it functions as an overflow barrier, thereby improving horizontal transfer. Regarding claim 2, the Office Action states that APA as modified by Hojo et al. teaches dopant density of the semiconductor region where the output transistor is formed is lower in a surface region rather than in the

middle region along the depth direction of the semiconductor substrate. Regarding claims 3 and 4, the Office Action states that APA as modified by Hojo et al. teaches the charge transfer element further comprising a load transistor (Ta1) serially connected to the output transistor and wherein the load transistor is formed in the semiconductor region (26) where the output transistor is formed.

Applicant has carefully reviewed Hojo et al. and notes that such reference discloses a technique of introducing a dopant in the P-Well region constituting the horizontal shift register so as to control the potential barrier. However, contrary to what is asserted in the Office Action, Hojo et al. nowhere describes the P-Well region having the maximum dopant density value in its middle region along the depth direction. Figs. 3-5 of Hojo et al. merely show potential distributions, and fail to illustrate any dopant density distributions. It should be noted that, for example, even when the dopant density in the P-Well region is uniform, a potential distribution having an increased value in the middle portion may be exhibited within the P-Well region as shown in Figs. 3-5 of Hojo et al. because the extent of the depletion layer is limited.

Further, although the Examiner contends that it would have been obvious to one skilled in the art to incorporate the teachings of Hojo et al. into APA so as to allow the P-Well region to function as an overflow barrier to thereby improve horizontal transfer, it is not an object of the present invention to control the overflow barrier of a horizontal shift register. The main object of the present invention is to stabilize the threshold voltage Vth of the gate of the output transistor for obtaining output from the horizontal shift register. The dopant density under the gate of the output transistor is adjusted for this purpose.

Claim 1 defines a charge transfer element which includes a reverse conductive type semiconductor region, a channel region of one conductive type, a

plurality of transfer electrodes, a capacitor formed continuous from the channel region, and an output transistor having a source and drain. Claim 1 further recites "the semiconductor region where the output transistor is formed exhibits an dopant density profile in a depth direction of the semiconductor substrate, which has a maximum dopant density value relative to a middle region of the semiconductor region". As such, claim 1 is submitted to clearly distinguish patentably over the attempted combination of APA and Hojo et al.

Claims 2-4 depend, directly or indirectly from, and contain all of the limitations of claim 1, so that such claims are also submitted to clearly distinguish patentably over the art.

In conclusion, claims 1-4 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

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By: _____

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